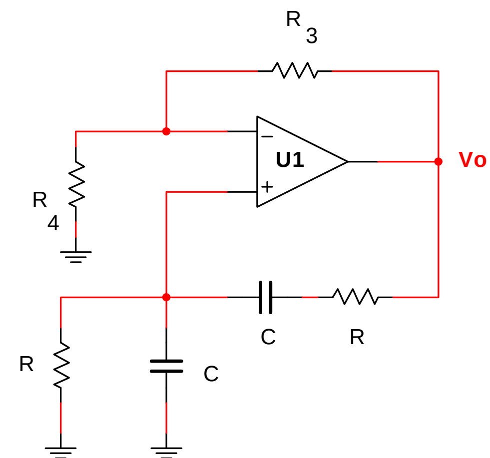
Wien Bridge Oscillator

Wien Bridge Oscillator



$f_o := 10.28\,kHz$ $\qquad j := \sqrt{-1}$

Will oscillate at frequency

$$f_o = \frac{1}{2\pi RC}$$

Pick $C := 1nF$

$$R := \frac{1}{2\cdot\pi\cdot C\cdot f_o} = 15.482\,k\Omega$$

if

$$1 + \frac{R_3}{R_4} = 3$$

Pick $R := 15k\Omega$

which is a standard value

Pick $R_3 := 20k\Omega$ $\qquad R_4 := 10k\Omega$

Page 170 of Lab Manual

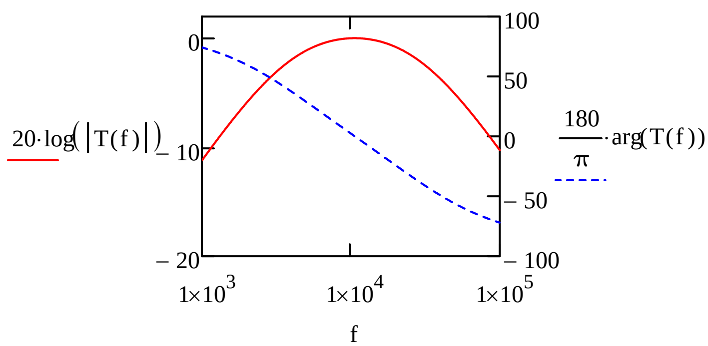
$R_1 = R_2 = R$ $\qquad C_1 = C_2 = C$

Transfer Function for Circuit shown in Fig 9.2.b

$$T(s) = \frac{V_o}{V_i} = \left(1 + \frac{R_3}{R_4}\right)\cdot\frac{sRC}{s^2 R^2 C^2 + 3sRC + 1}$$

Second Order BPF

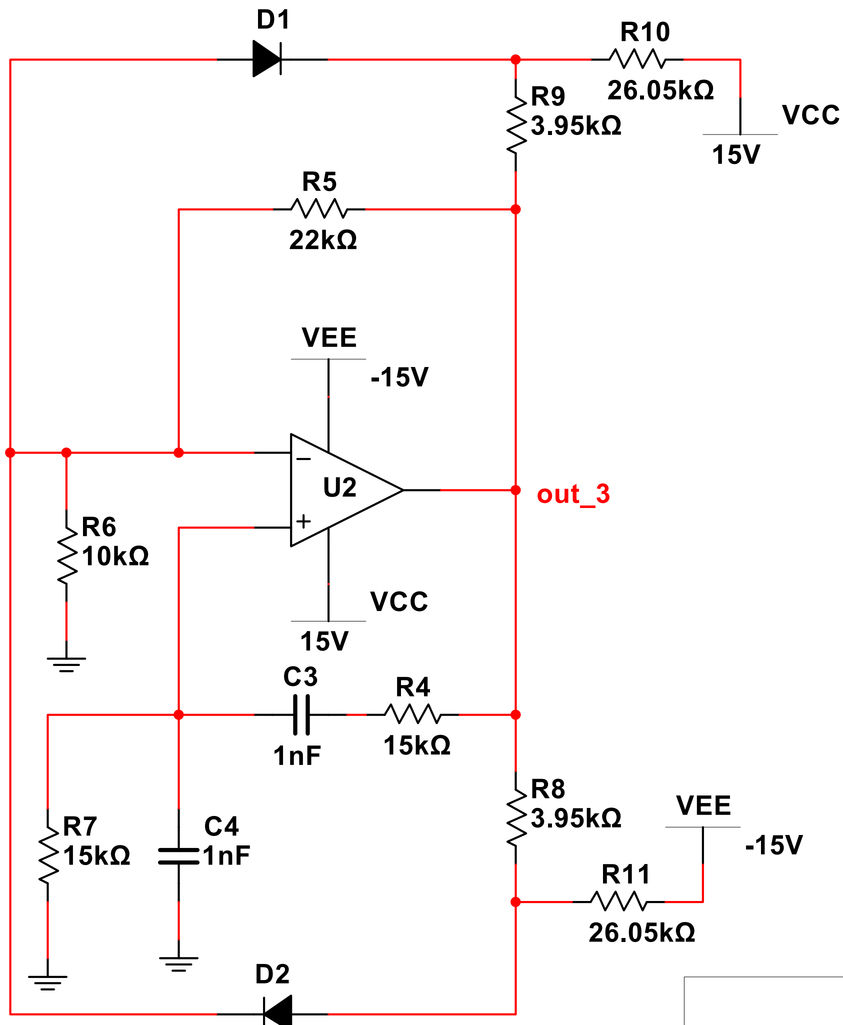
$$T(f) := \left(1 + \frac{R_3}{R_4}\right)\cdot\frac{j\cdot 2\cdot\pi\cdot f\cdot R\cdot C}{(j\cdot 2\cdot\pi\cdot f\cdot R\cdot C)^2 + 3\cdot(j\cdot 2\cdot\pi\cdot f\cdot R\cdot C) + 1}$$

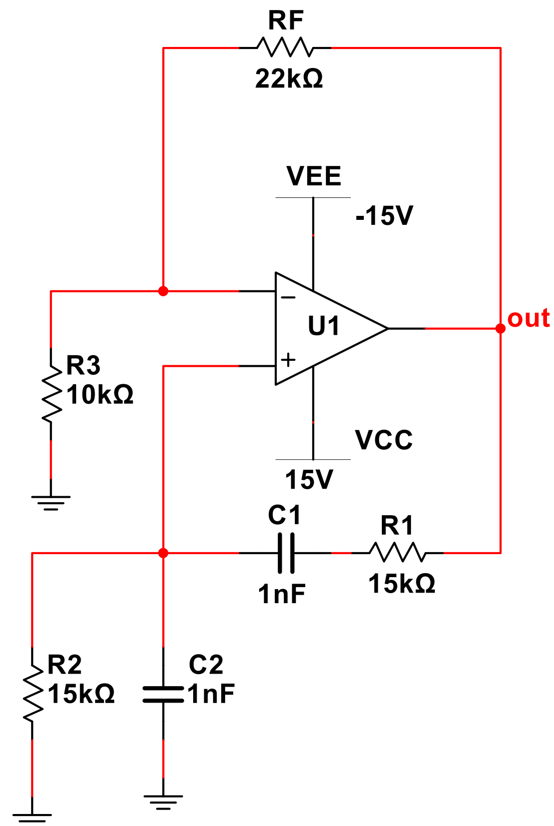


For the diode limiter network pick $\qquad R_A + R_B = 30k\Omega \qquad V_\gamma = 0.7V$

$|V_o| = 5V$ $\qquad$ the peak value of the output sine wave. Solution with Eqn 9.8 yields

$R_A = 3.95k\Omega$ $\qquad R_B = 26.05k\Omega$



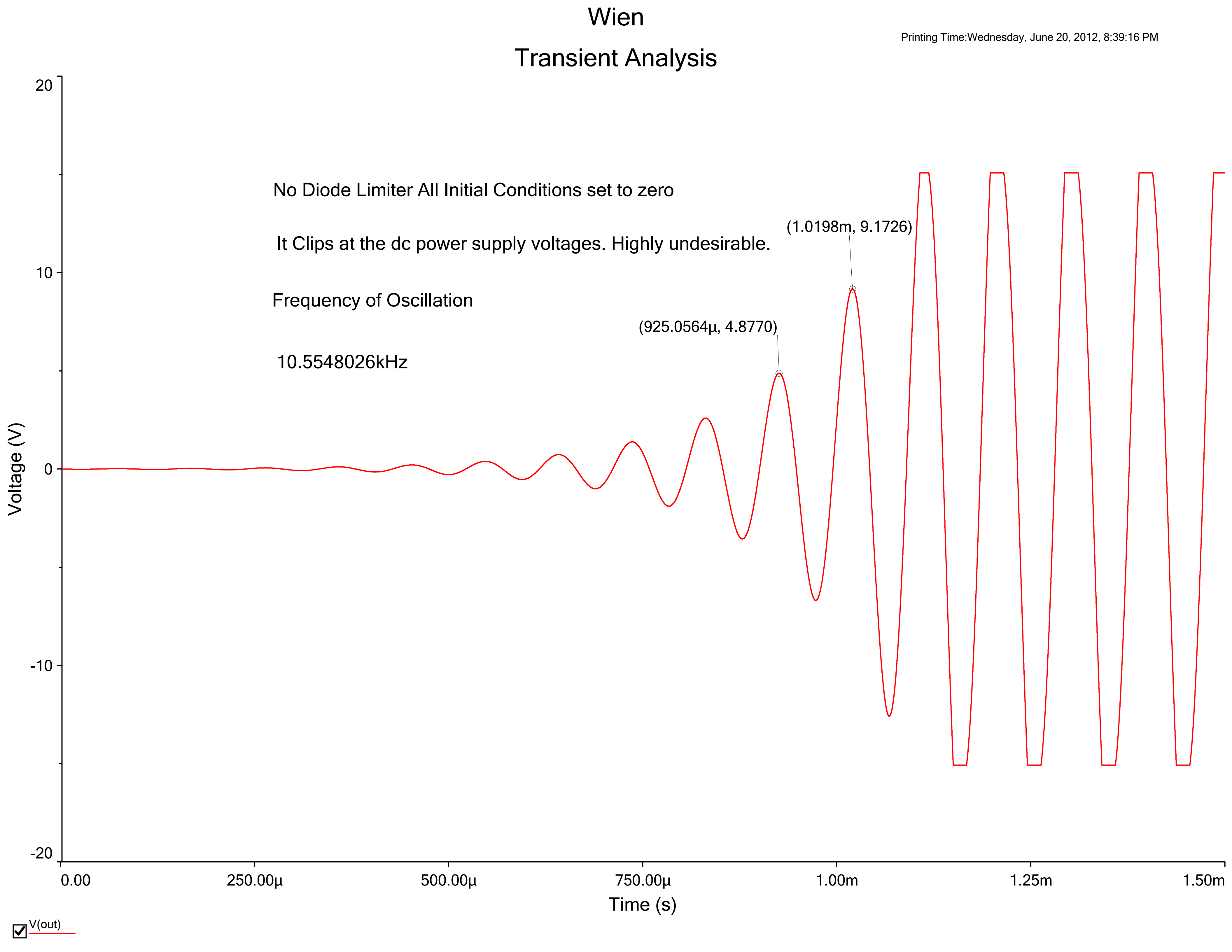


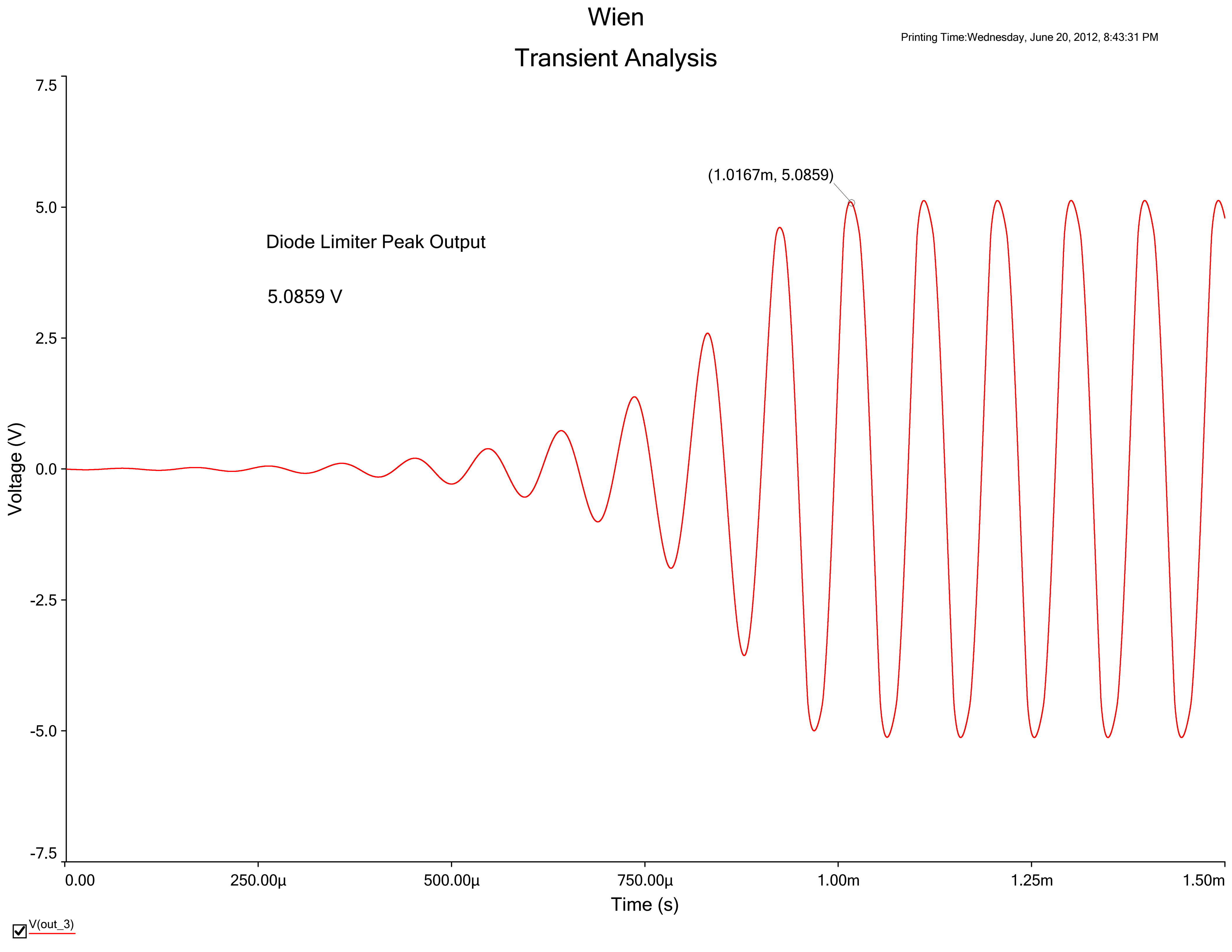
Title: Wien		
Size: A	Document N: 0001	Revision: 1.0
Date: 2012-06-20	Sheet 1 of 1	

Set ICs to Zero and use small time steps compared to a period.

Use Virtual Op Amp 5 Terminals

This is Multisim


Wien
Transient Analysis
Printing Time:Wednesday, June 20, 2012, 8:39:16 PM
No Diode Limiter All Initial Conditions set to zero
It Clips at the dc power supply voltages. Highly undesirable.
Frequency of Oscillation
10.5548026kHz
(1.0198m, 9.1726)
(925.0564µ, 4.8770)
20
10
0
-10
-20
Voltage (V)
0.00
250.00µ
500.00µ
750.00µ
1.00m
1.25m
1.50m
Time (s)
V(out)

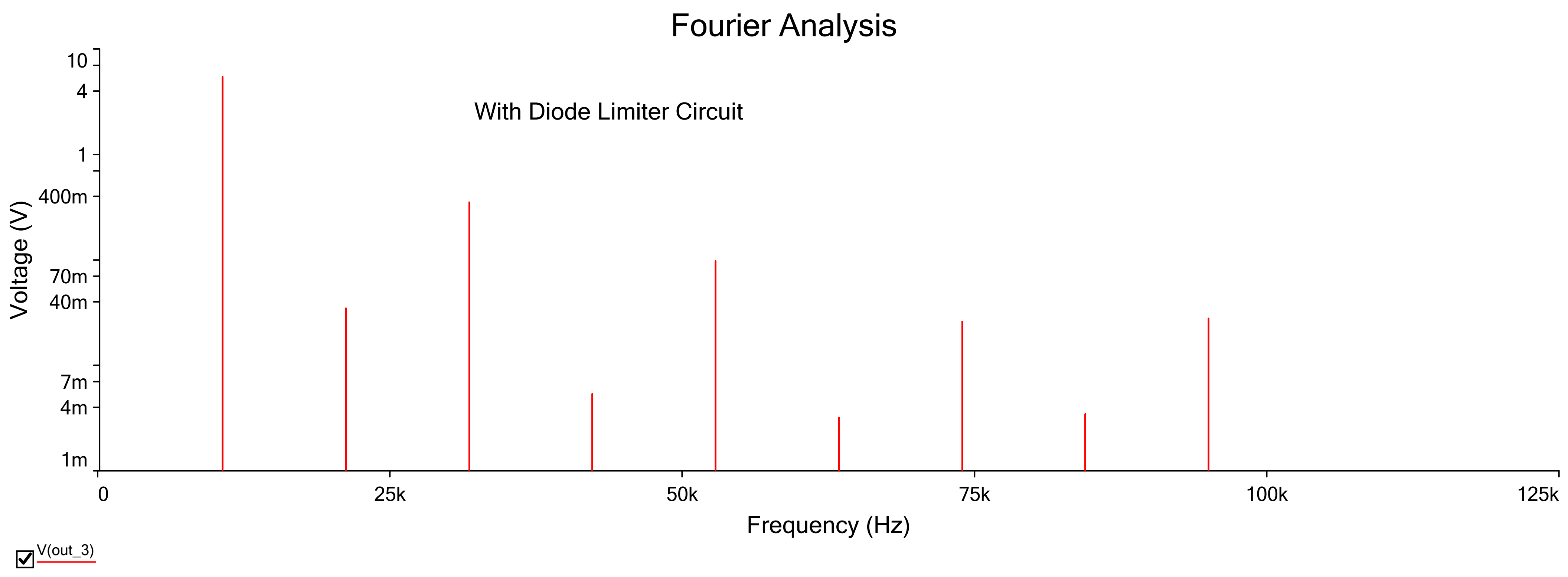


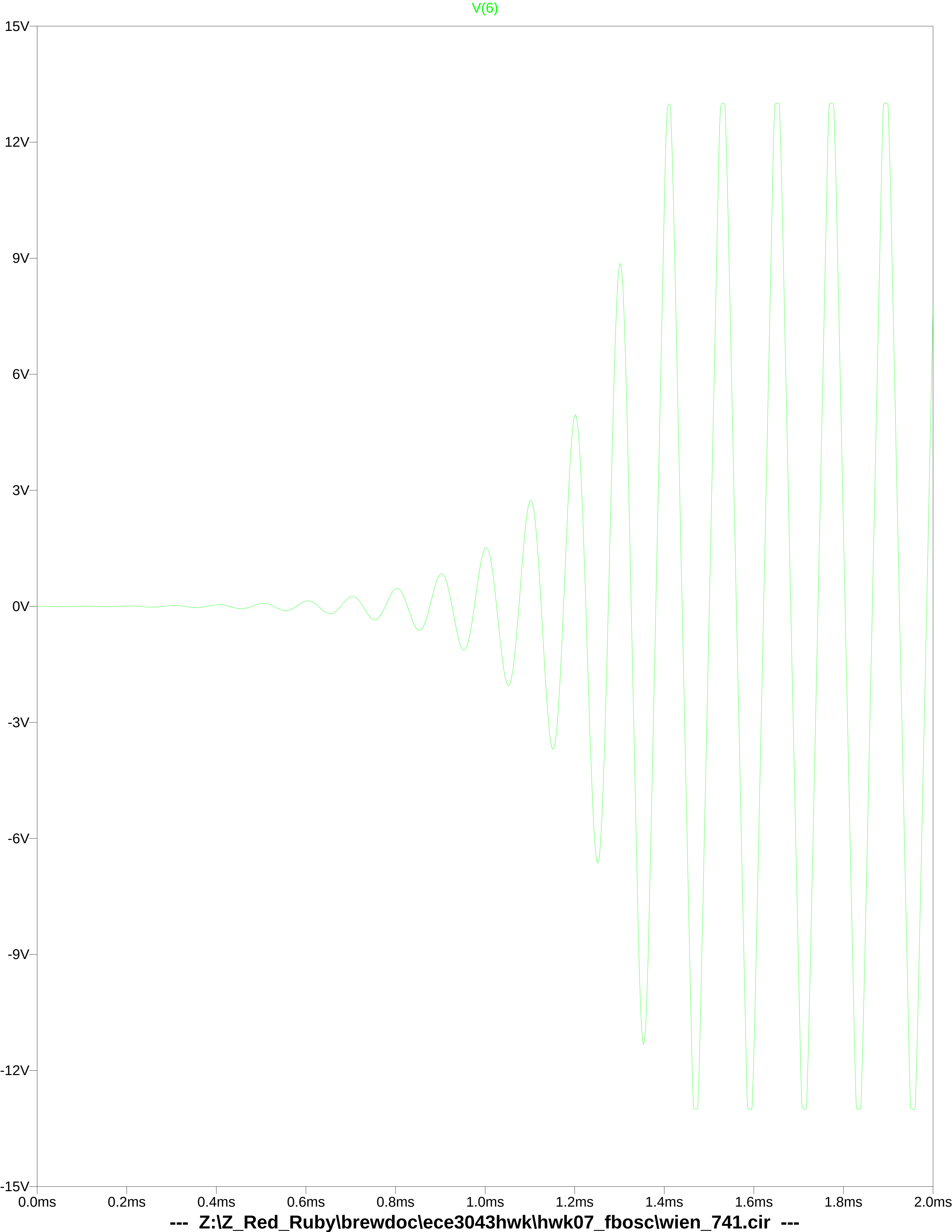
Wien
Transient Analysis
Printing Time:Wednesday, June 20, 2012, 8:43:31 PM
(1.0167m, 5.0859)
Diode Limiter Peak Output
5.0859 V
7.5
5.0
2.5
0.0
-2.5
-5.0
-7.5
Voltage (V)
0.00
250.00µ
500.00µ
750.00µ
1.00m
1.25m
1.50m
Time (s)
V(out_3)

Wien

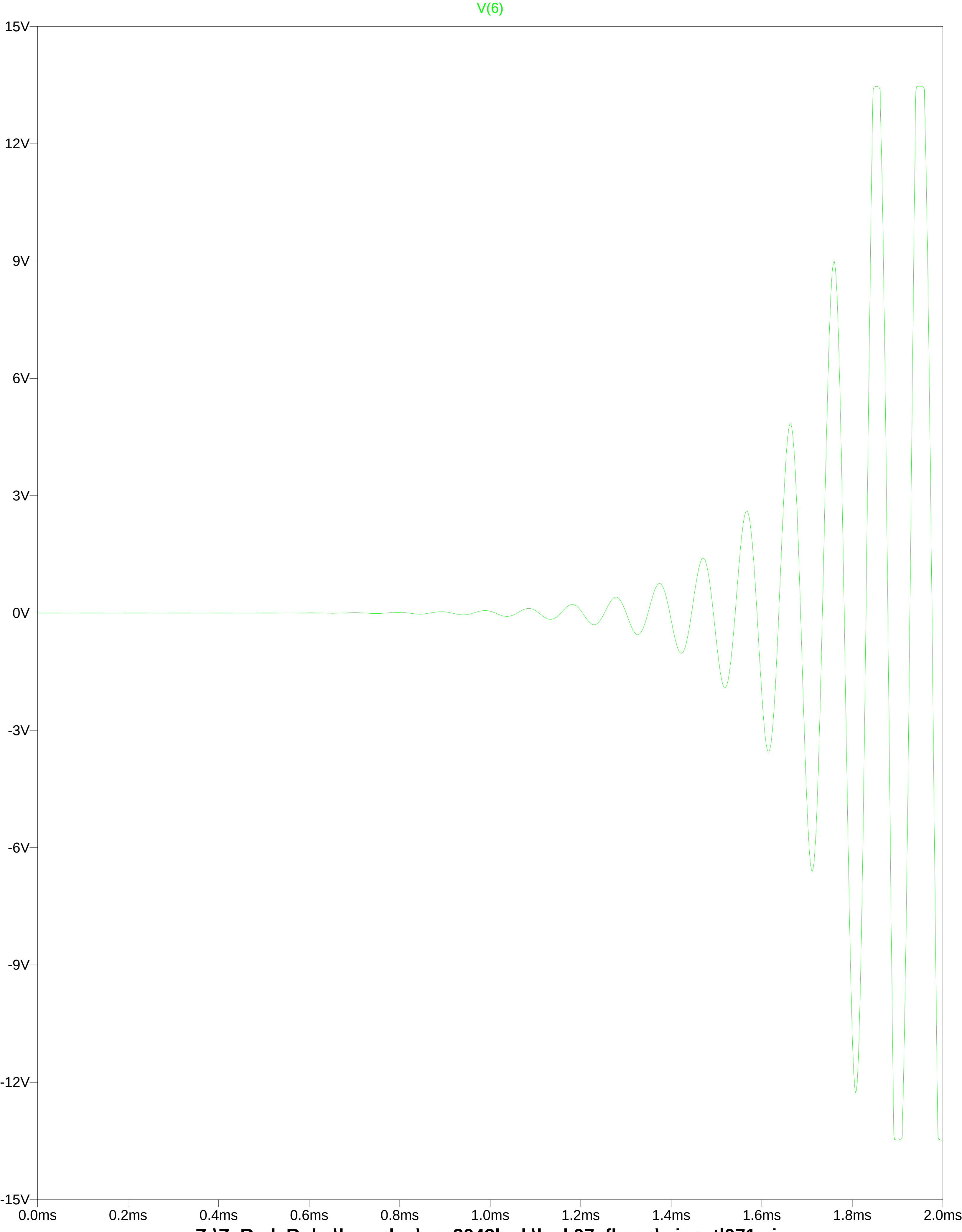
Printing Time:Wednesday, June 20, 2012, 8:49:20 PM

1	Fourier analysis for V(out_3):					
2	DC component:	-0.031584				
3	No. Harmonics:	9				
4	THD:	6.76763 %				
5	Grid size:	256				
6	Interpolation Degree:	1				
7						
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	1	10554.8	5.44243	112.088	1	0
10	2	21109.6	0.0346508	125.259	0.00636679	13.1715
11	3	31664.4	0.351388	-55.842	0.0645646	-167.93
12	4	42219.2	0.00535184	-155.24	0.000983356	-267.33
13	5	52774	0.0974462	31.9446	0.0179049	-80.143
14	6	63328.8	0.00318635	68.2141	0.000585465	-43.874
15	7	73883.6	0.0258589	-154.2	0.00475135	-266.29
16	8	84438.4	0.0034441	153.858	0.000632825	41.7704
17	9	94993.2	0.0277988	-48.781	0.0051078	-160.87
18						




V(6)
15V
12V
9V
6V
3V
0V
-3V
-6V
-9V
-12V
-15V
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
--- Z:\Z_Red_Ruby\brewdoc\ece3043hwk\hwk07_fbosc\wien_741.cir ---

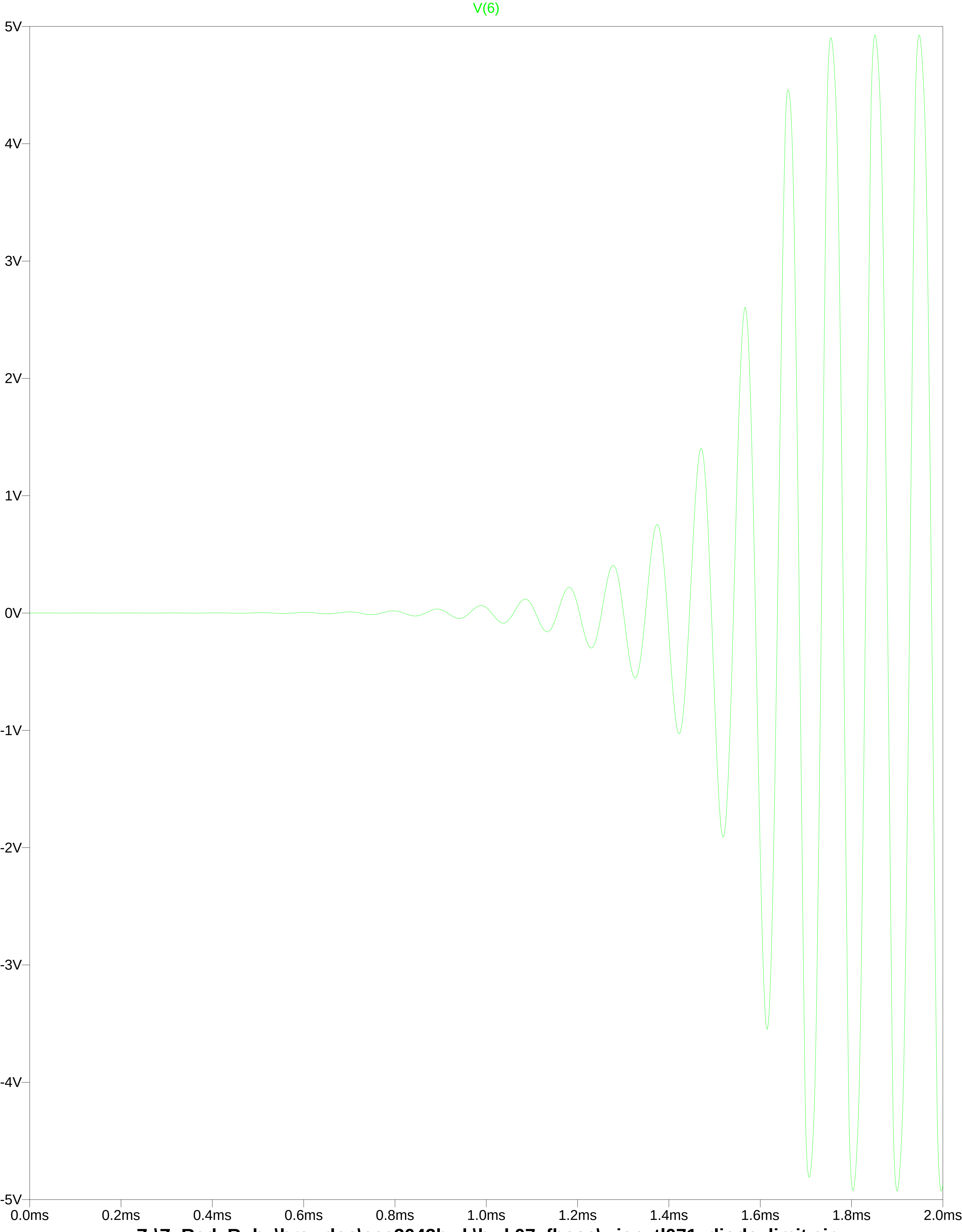
```
Wien Bridge Oscillator
*No Diode Amplitude Limiter
Cp 3 0 1n IC=0
Rp 3 0 15k
Cs 3 36 1n IC=0
Rs 36 6 15k
R1 2 0 10k
R2 2 6 22k
X0A 3 2 7 4 6 TL071
VCC 7 0 DC 15
VEE 4 0 DC -15
* TL071 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.01 ON 06/16/89 AT 13:08
* (REV N/A)      SUPPLY VOLTAGE: +/-15V
* CONNECTIONS:   NON-INVERTING INPUT
*                | INVERTING INPUT
*                | | POSITIVE POWER SUPPLY
*                | | | NEGATIVE POWER SUPPLY
*                | | | | OUTPUT
*                | | | | |
.SUBCKT TL071    1 2 3 4 5
*
  C1   11 12 3.498E-12
  C2    6  7 15.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 4.715E6 -5E6 5E6 5E6 -5E6
  GA    6  0 11 12 282.8E-6
  GCM   0  6 10 99 8.942E-9
  ISS   3 10 DC 195.0E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 3.536E3
  RD2   4 12 3.536E3
  RO1   8  5 150
  RO2   7 99 150
  RP    3  4 2.143E3
  RSS  10 99 1.026E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC 2.200
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=15.00E-12 BETA=270.1E-6 VTO=-1)
.ENDS TL071
.TRAN 0 2m UIC
.PROBE
.END
```



--- Z:\Z_Red_Ruby\brewdoc\ece3043hwk\hwk07_fbosc\wien_tl071.cir ---

```
Wien Bridge Oscillator
*With Diode Amplitude Limiter
Cp 3 0 1n IC=0
Rp 3 0 15k
Cs 3 36 1n IC=0
Rs 36 6 15k
R1 2 0 10k
R2 2 6 22k
X0A 3 2 7 4 6 TL071
VCC 7 0 DC 15
VEE 4 0 DC -15
D1 2 8 d1n4148
D2 9 2 d1n4148
Ra 6 8 3.95k
Rb 8 7 26.05k
Ra1 6 9 3.95k
Rb1 9 4 26.05k
.model d1n4148 D(is=1n bv=100 n=1.8)
* TL071 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.01 ON 06/16/89 AT 13:08
* (REV N/A)      SUPPLY VOLTAGE: +/-15V
* CONNECTIONS:   NON-INVERTING INPUT
*                | INVERTING INPUT
*                | | POSITIVE POWER SUPPLY
*                | | | NEGATIVE POWER SUPPLY
*                | | | | OUTPUT
*                | | | | |
.SUBCKT TL071    1 2 3 4 5
*
  C1   11 12 3.498E-12
  C2    6  7 15.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 4.715E6 -5E6 5E6 5E6 -5E6
  GA    6  0 11 12 282.8E-6
  GCM   0  6 10 99 8.942E-9
  ISS   3 10 DC 195.0E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 3.536E3
  RD2   4 12 3.536E3
  RO1   8  5 150
  RO2   7 99 150
  RP    3  4 2.143E3
  RSS  10 99 1.026E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC 2.200
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=15.00E-12 BETA=270.1E-6 VTO=-1)
.ENDS TL071
.TRAN 0 2m UIC
.PROBE
```

.END



--- Z:\Z_Red_Ruby\brewdoc\ece3043hwk\hwk07_fbosc\wien_tl071_diode_limit.cir ---

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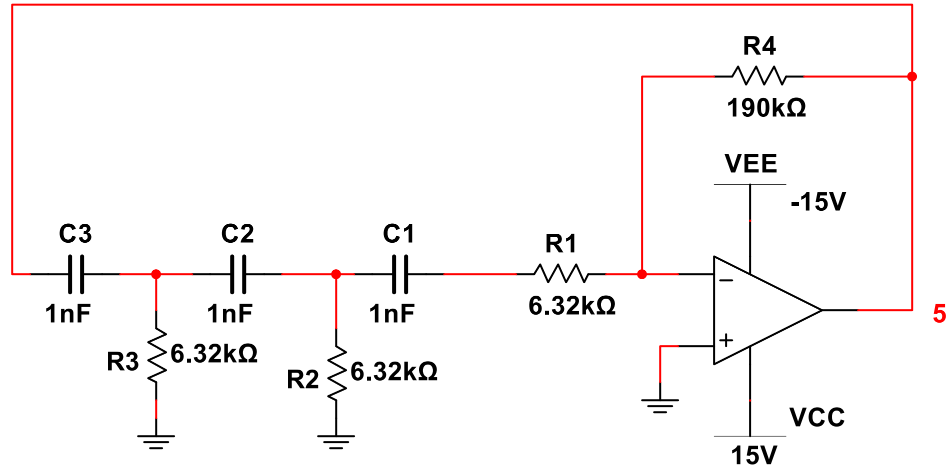
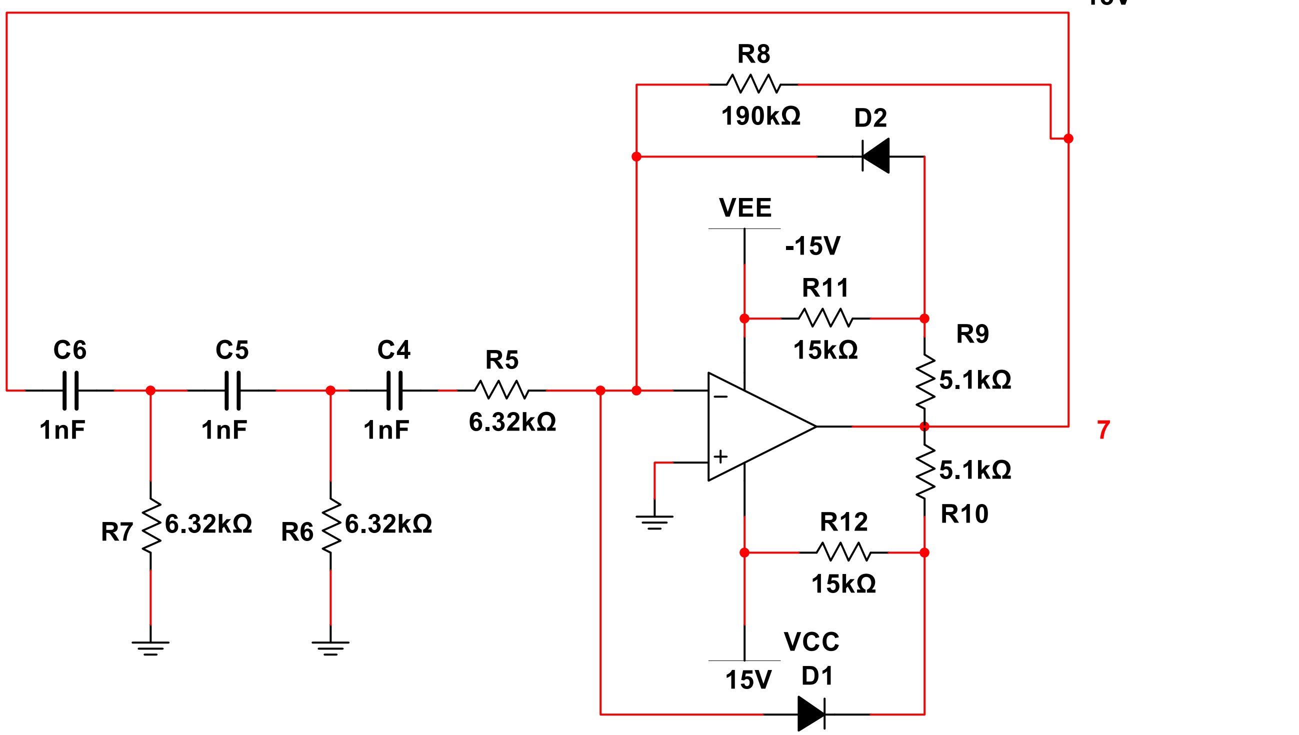
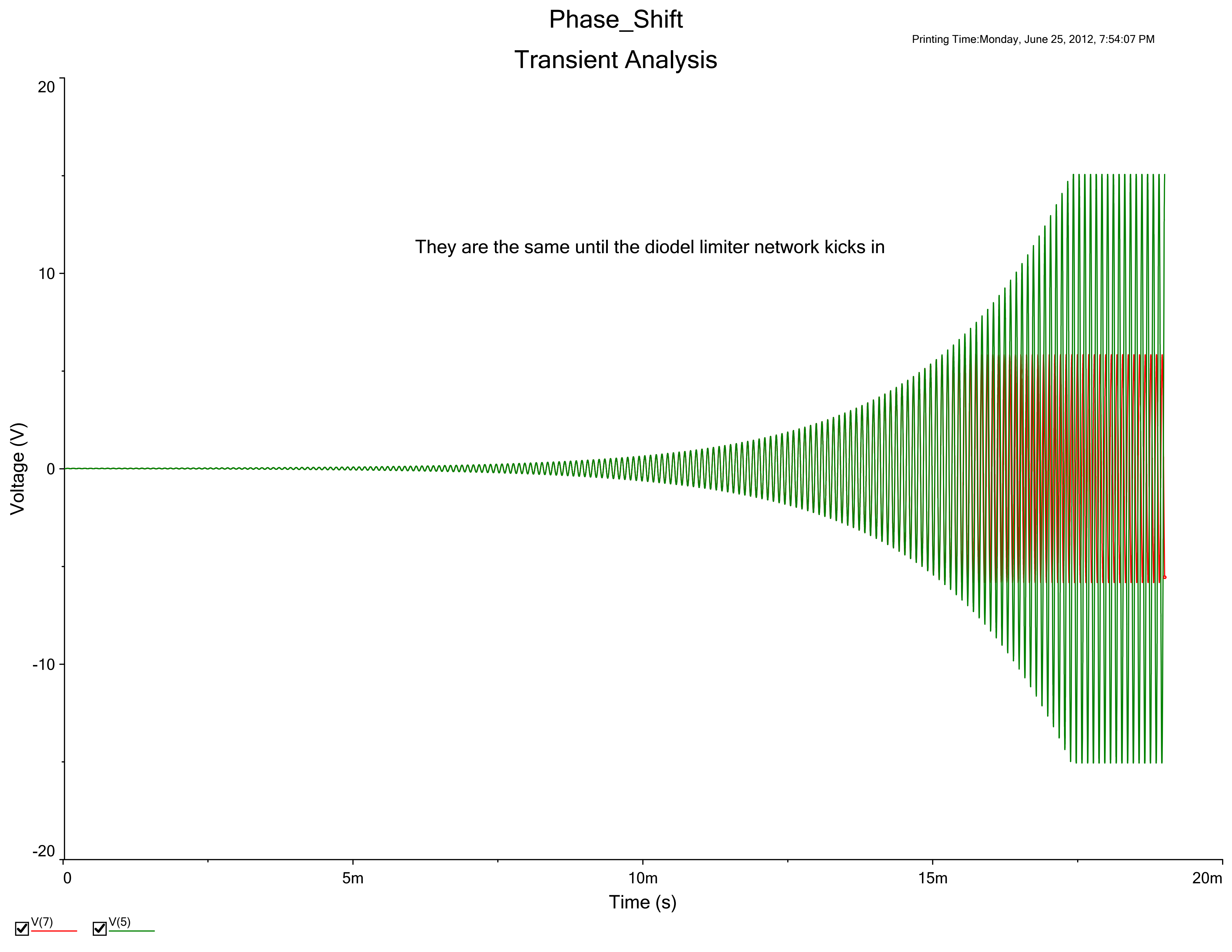
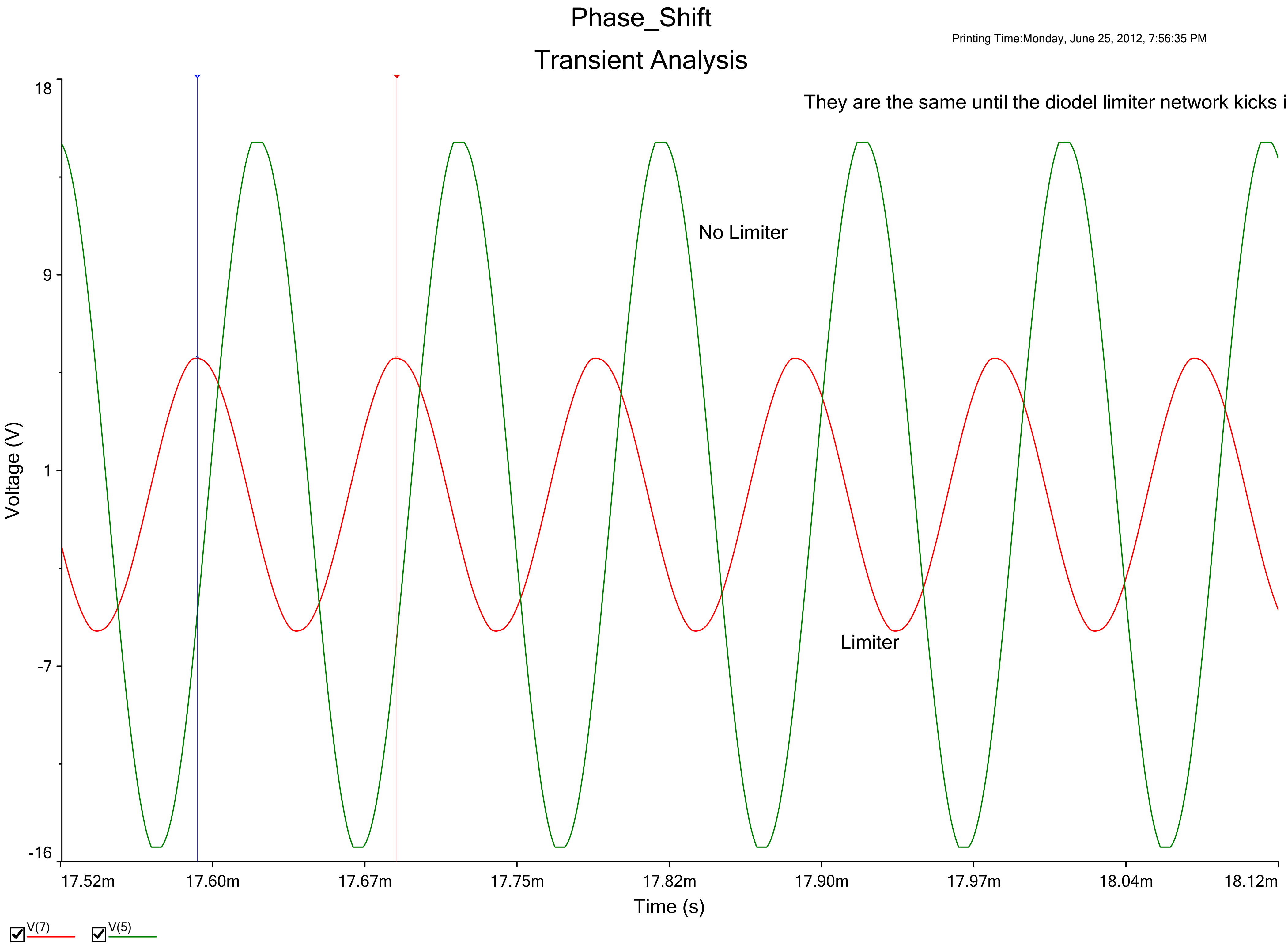
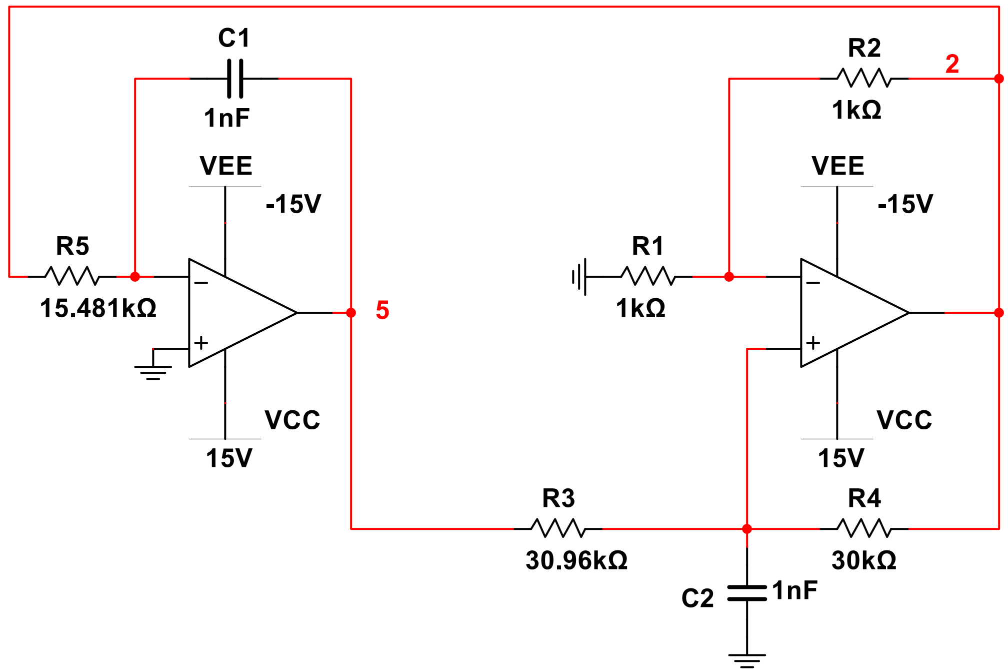





Phase_Shift
Printing Time:Monday, June 25, 2012, 7:54:07 PM
Transient Analysis
They are the same until the diodel limiter network kicks in
20
10
0
-10
-20
Voltage (V)
0
5m
10m
15m
20m
Time (s)
V(7)
V(5)



	x1	y1	x2	y2	dx	dy	dy/dx	1/dx
V(7):	17.6883m	5.8314	17.5909m	5.8308	-97.4169µ	-615.3424µ	6.3166	-10.2652k
V(5):	17.6883m	-6.1310	17.5909m	-5.0948	-97.4169µ	1.0362	-10.6366k	-10.2652k



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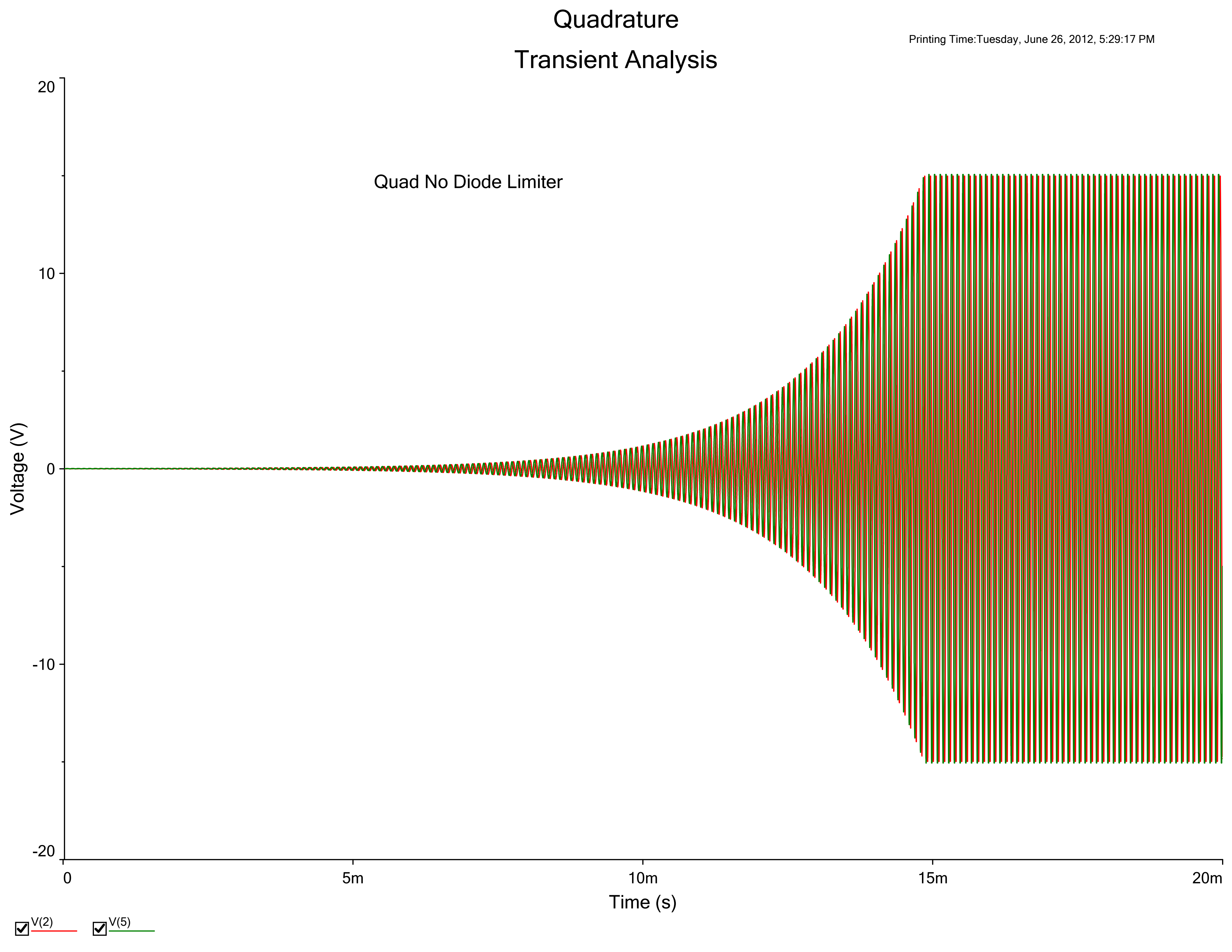
Quadrature Oscillator No Diode Limiter

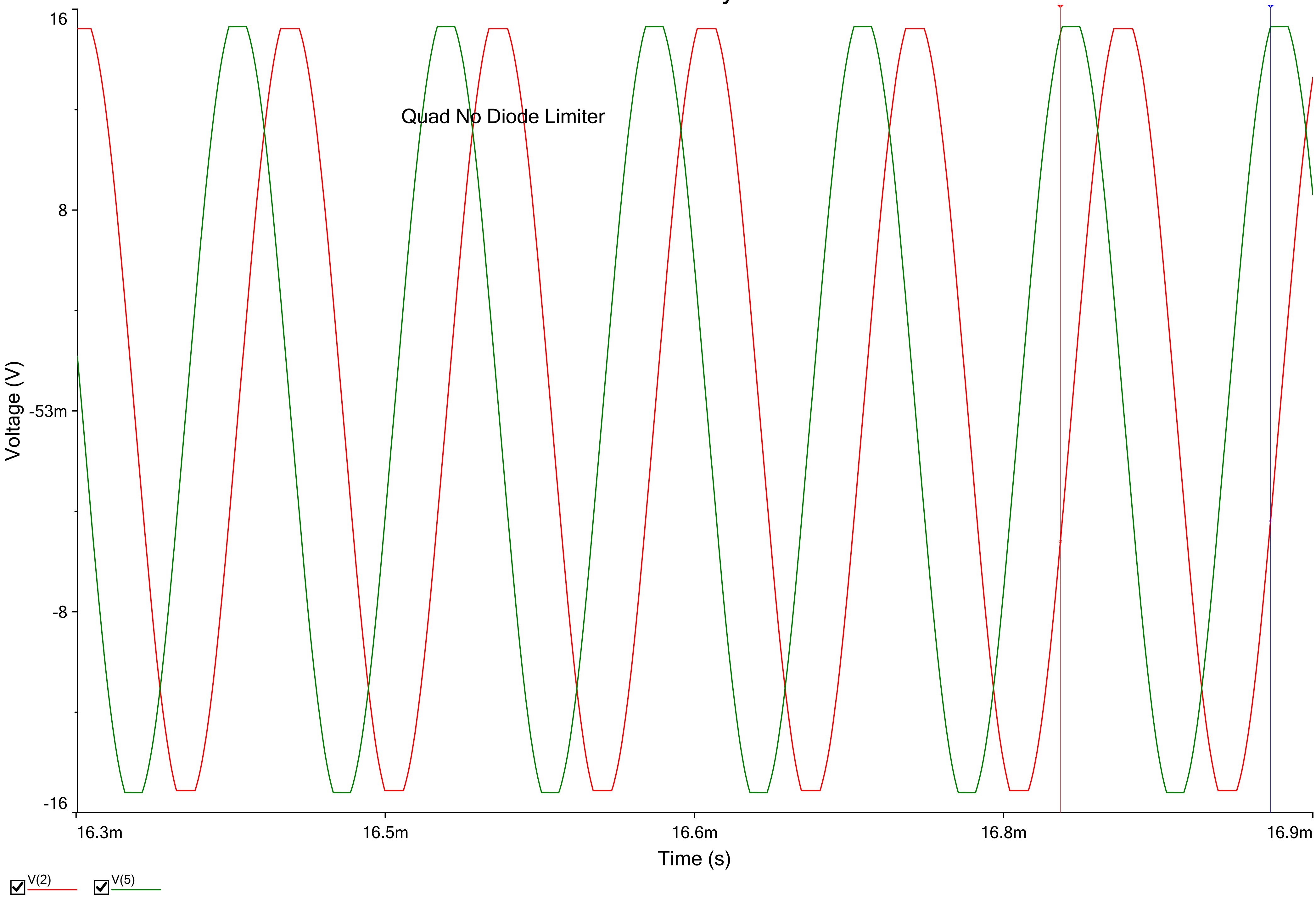


Quadrature
Printing Time:Tuesday, June 26, 2012, 5:29:17 PM
Transient Analysis
Quad No Diode Limiter
20
10
0
-10
-20
Voltage (V)
0
5m
10m
15m
20m
Time (s)
V(2)
V(5)

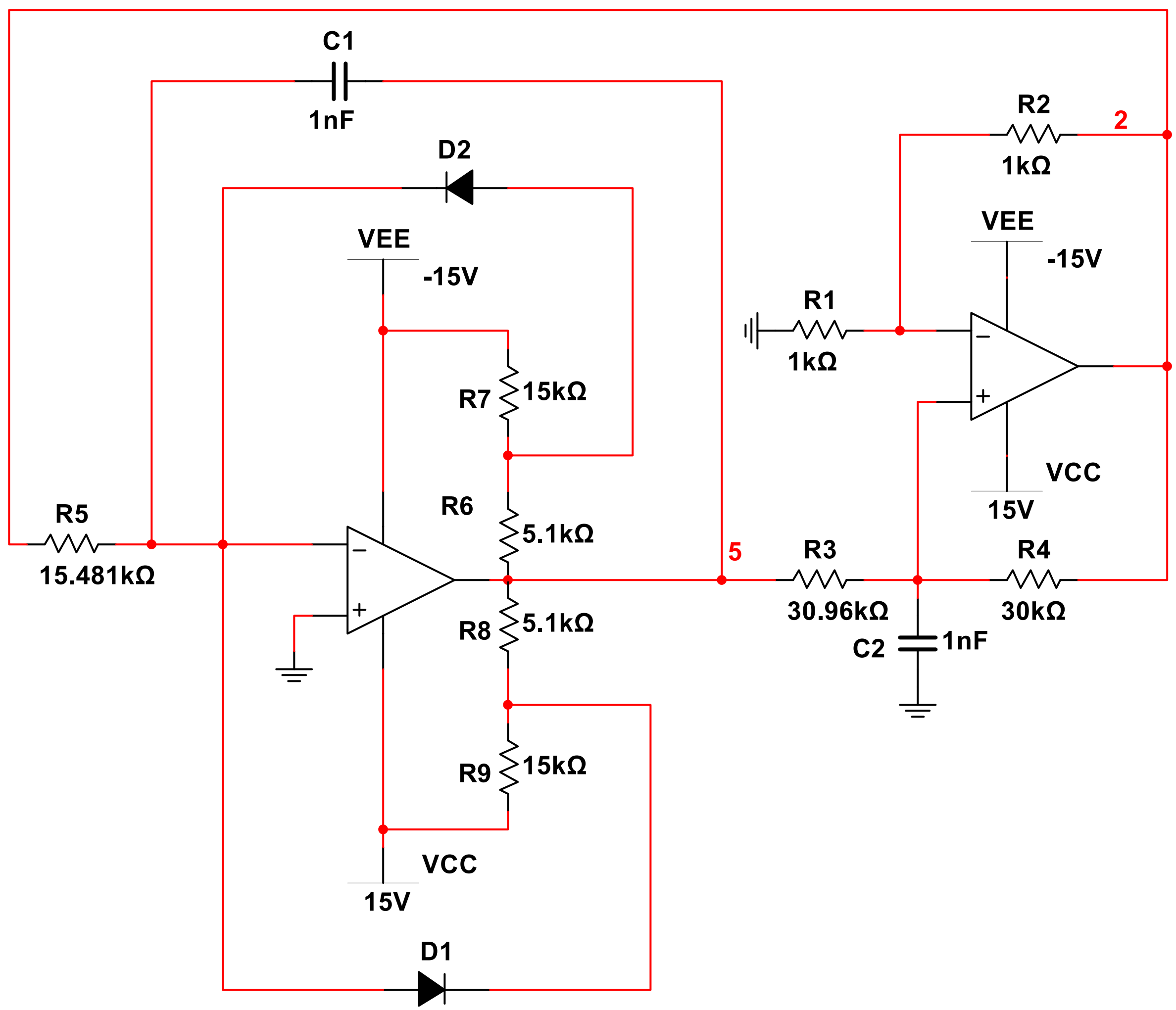
Quadrature

Transient Analysis

Printing Time:Tuesday, June 26, 2012, 5:30:54 PM



	x1	y1	x2	y2	dx	dy	dy/dx	1/dx
V(2):	16.7871m	-5.1974	16.8860m	-4.3953	98.9405µ	802.0629m	8.1065k	10.1071k
V(5):	16.7871m	14.7697	16.8860m	15.0293	98.9405µ	259.6381m	2.6242k	10.1071k



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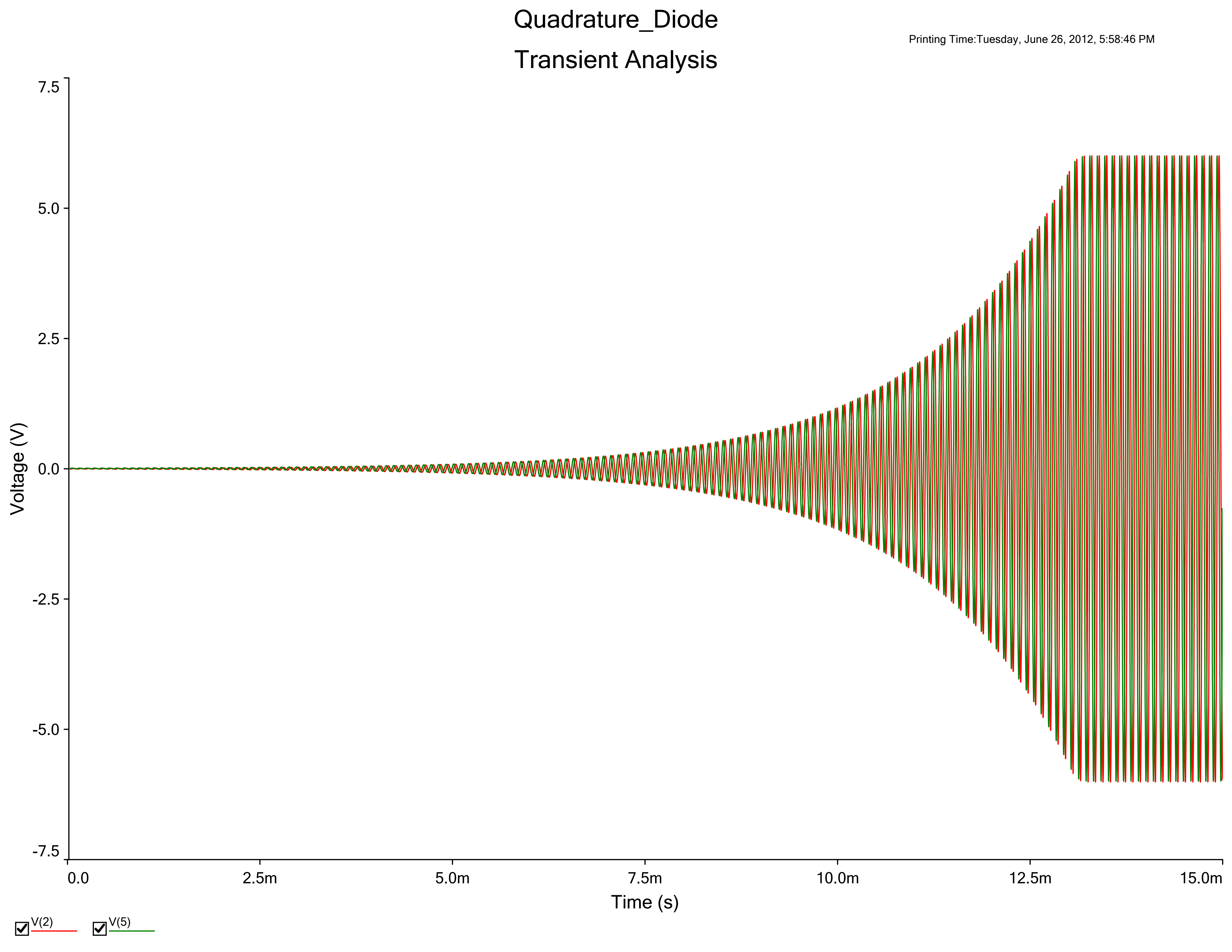
Quadrature Oscillator with Diode Limiter

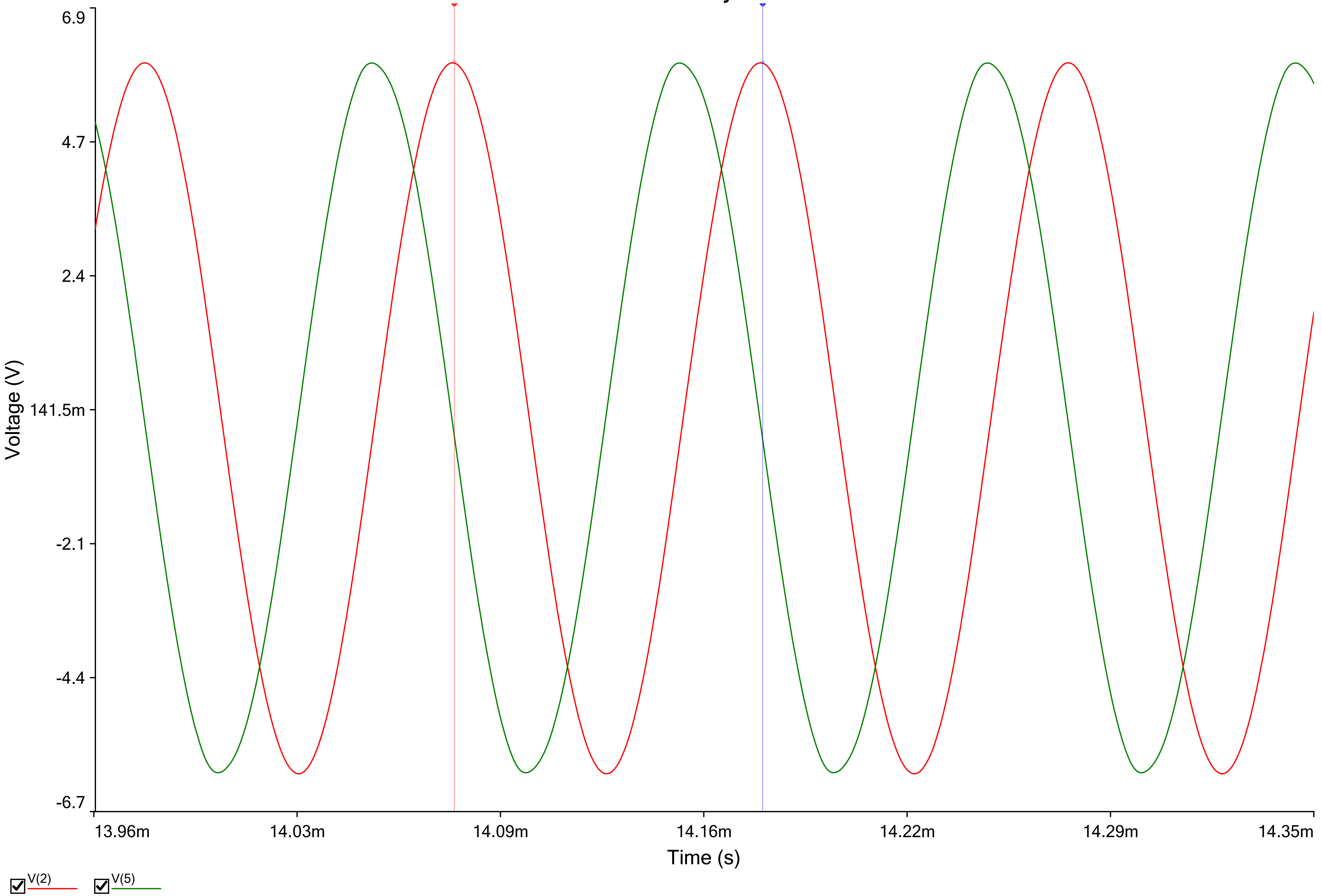


Quadrature_Diode
Printing Time:Tuesday, June 26, 2012, 5:58:46 PM
Transient Analysis
Voltage (V)
7.5
5.0
2.5
0.0
-2.5
-5.0
-7.5
0.0
2.5m
5.0m
7.5m
10.0m
12.5m
15.0m
Time (s)
V(2)
V(5)

Quadrature_Diode

Transient Analysis

Printing Time:Tuesday, June 26, 2012, 6:00:12 PM



	x1	y1	x2	y2	dx	dy	dy/dx	1/dx
V(2):	14.0782m	6.0018	14.1757m	5.9989	97.5181µ	-2.8724m	-29.4549	10.2545k
V(5):	14.0782m	-292.1749m	14.1757m	-364.8312m	97.5181µ	-72.6563m	-745.0549	10.2545k

Georgia Institute of Technology

School of Electrical and Computer Engineering

ECE 3043 Electrical and Electronic Circuits Laboratory Verification Sheet

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NAME:____ SECTION:____________________________

AD LOGIN:___________________________________

Experiment 9: Linear Op-Amp Oscillators

Procedure	Time Completed	Date Completed	Verification (Must demonstrate circuit)	Points Possible	Points Received
3. Wein Bridge				25	
4. Phase Shift				25	
5. Quadrature				25	

Enter your critical frequency below:

f_{crit}	

To be permitted to complete the experiment during the open lab hours, you must complete at least **three** procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE:____________________________________ DATE:_____________________________________

ECE 3043 Check-off Requirements for Experiment 9

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

Wein bridge and phase shift oscillators

- ✓ Scope capture showing open loop input and output waveforms in phase. Display Vpp and frequency measurements.
- ✓ Scope capture showing closed loop output waveform. Display Vpp and frequency measurements.
- ✓ Scope capture showing closed loop output waveform with limiter. Display Vpp and frequency measurements.
- ✓ Comparison of the measured frequency of oscillation to the design value. Adjust the circuit component values if the measured value is not within 10% of the design value.

Quadrature oscillator

- ✓ Scope capture showing both output waveforms. Display Vpp, frequency, and phase measurements.
- ✓ Scope capture of XY plot.
- ✓ Comparison of the measured frequency of oscillation to the design value. Adjust the circuit component values if the measured value is not within 10% of the design value.